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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,448	04/01/2004	Soon-Hong Ahn	8021-227 (SS-19246-US)	7782

22150 7590 10/13/2005

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/815,448	AHN ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 6-10, 19, 23-24 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 6690067 to Ker et al.

Regarding claim 1, Ker discloses a semiconductor device in fig. 3b comprising: a first well (left N-well) connected to a pad, fig. 3b, to which an external pin is connected, the first well including a first-type diffusion region N+ that receives a well bias voltage, a second well adjacent to the first well, a second well (second well comprises P-substrate in both side of middle N-well) including an insulating region (middle N-well) and at least one second-type diffusion region P+ outside the insulating region, fig. 3b; and a third well (right N-well) adjacent to the second well and including a first-type diffusion region N+ that receives a first voltage, fig. 3b, wherein the insulating region inside the second well along with the first-type diffusion N+ region of the first well constitute a bipolar junction transistor, which cuts off current flowing from the first well to the third well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure recited in the Ker's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

With respect to second well, the substrate is a P-type substrate, i.e. lightly dope; thus substrate would be interpreted a well.

Regarding claim 2, Ker discloses the semiconductor device, wherein the at least one second-type diffusion region outside the insulating region comprises a first second-type diffusion region and a second second-type diffusion region, and the second well comprises: a first sub-well arranged (P-substrate) between the insulating region (middle N-well) and the first well (left N-well) and including the first second-type diffusion region P+; and a second sub-well arranged between (P-substrate) the insulating region and the third well (right N-well) and including the second second-type diffusion region P+, wherein the insulating region (middle N-well) is a third sub-well having a first-type diffusion region (N).

Regarding claim 3, Kerr discloses the semiconductor device wherein the first and second sub-wells (left and right P-substrate portions of middle N-well) of the second

well are P-wells, and the first voltage is applied to the second-type diffusion regions of the first and second sub-wells of the second well, fig. 3b

Regarding claim 4, Kerr discloses the semiconductor device wherein the third sub-well (right N-well) is an N-well, and a second voltage is applied to the first-type diffusion region of the third sub-well, fig. 3b.

Regarding claim 5, Kerr discloses the semiconductor device wherein the first voltage is a ground voltage, and the second voltage generates a backward voltage between a base and an emitter of a bipolar junction transistor, the bipolar junction transistor comprising the first-type diffusion region N+ of the first well, the second-type diffusion region P+ of the first sub-well, and the first-type diffusion region N+ of the third sub-well.

Regarding claim 6, Kerr discloses the semiconductor device wherein the first (left N-well) and third wells (right N-well) are N-wells, fig. 3b.

Regarding claim 7, Kerr discloses the semiconductor device wherein the well bias voltage applied to the first-type diffusion region N+ of the first well is a power supply voltage, fig. 3b

Regarding claim 8, Ker discloses the semiconductor device wherein a region to which the pad is connected is a second-type diffusion region P+, fig. 3b.

Regarding claim 9, Kerr discloses the semiconductor device wherein the first-type diffusion regions are formed of N-type impurities, and the at least one second-type diffusion region is formed of P-type impurities, fig. 3b

Regarding claim 10, Kerr discloses the semiconductor device wherein the insulating region (middle N-well) of the second well has a structure that surrounds the first well to view in fig. 3b.

Regarding claim 12, Kerr discloses a semiconductor device in fig. 3b comprising: a first N-well connected to a pad to which an external pin is connected, the first N-well (left N-well) including an N-type diffusion region N+ that receives a well bias voltage, and a P-type diffusion region P+, fig. 3b, formed in the vicinity of the pad; a first P-well (P-substrate) adjacent to the first N-well, the first P-well including an insulating region (middle N-well) and at least one P-type diffusion region P+ that receives a ground voltage outside the insulating region; and a second N-well (right N-well) adjacent to the first P-well and including an N-type diffusion region N+ that receives the ground voltage, wherein the insulating region is a third N-well (middle N-well) having an N-type diffusion region N+ that receives a control voltage, fig. 3b.

Regarding claim 13, Kerr discloses the semiconductor device wherein the at least one P-type diffusion region P+ comprises a first P-type diffusion region P+ and a second P-type diffusion region P+, fig. 3b, and the first P-well comprises: a first sub-P-well (left P-substrate of middle N-well) located between the insulating region and the first N-well (left N-well) and including the first P-type diffusion region P+; and a second sub-P-well (right P-substrate of middle N-well) located between the insulating region and the second N-well (right N-well) and including the second P-type diffusion region P+.

Regarding claim 14, Kerr discloses the semiconductor device wherein the N-type diffusion region of the first N-well, the P-type diffusion region of the first sub-P-well, and the N-type diffusion region of the insulating region constitute a bipolar junction transistor which cuts off a current flowing from the first N-well to the second N-well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure recited in the Ker's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 15, Kerr discloses the semiconductor device wherein the control voltage generates a backward voltage between a base and an emitter of the bipolar junction transistor composed of the N-type diffusion region of the first N-well, the P-type diffusion region of the first sub-P-well, and the N-type diffusion region of the insulating region.

With respect to 'a backward voltage between a base and an emitter of the bipolar junction transistor', the structure recited in the Ker's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by

identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 16, Kerr discloses the semiconductor device wherein the well bias voltage applied to the N-type diffusion region of the first N-well is a power supply voltage, fig. 3b.

Regarding claim 17, Kerr discloses the semiconductor device wherein the insulating region of the first P-well has a structure that surrounds the first N-well, fig. 3b.

Regarding claim 19, Kerr discloses a method of forming a semiconductor device comprising: forming a first well (left N-well) connected to a pad, fig. 3b, to which an external pin is connected, the first well including a first-type diffusion region N+ that receives a well bias voltage; forming a second well (second well comprises P-substrate in both side of middle N-well) adjacent to the first well, the second well including an insulating region (middle N-well) and at least one second-type diffusion region P+ outside the insulating region; and forming a third well (right N-well) adjacent to the second well and including a first-type diffusion region P+ that receives a first voltage, wherein the insulating region inside the second well along with the first-type diffusion region N+ of the first well constitute a bipolar junction transistor, fig. 3b, which cuts off current flowing from the first well to the third well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure

recited in the Kerr's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claims 20, 22, Kerr discloses the method wherein the at least one second-type diffusion region P+ outside the insulating region comprises a first second-type diffusion region N+ and a second second-type diffusion region P+, and the step of forming a second well comprises: forming a first sub-well (left P-substrate) between the insulating region (middle N-well) and the first well (left N-well), the first sub-well including the first second-type diffusion region p+; and forming a second sub-well (right P-substrate) between the insulating region and the third well (right N-well), the second sub-well including the second second-type diffusion region P+, wherein the insulating region having a first-type diffusion region N+, wherein the insulating region is a third sub N-well.

Regarding claim 21, Kerr discloses the method wherein the first and second sub-wells of the second well are P-wells (P-substrate), and the first voltage is applied to the second-type diffusion regions of the first and second sub-wells of the second well, fig. 3b.

Regarding claim 23, Kerr discloses the method wherein the first and third wells are N-wells (left and right N-well), fig. 3b.

Regarding claim 24, Kerr discloses the method wherein the first-type diffusion regions N+ are formed of N-type impurities, and the at least one second-type diffusion region P+ is formed of P-type impurities, fig. 3b.

3. Claims 1, 12, and 19 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 847059 to Tsuji et al.

Regarding claim 1, Tsuji discloses a semiconductor device in fig. 1 comprising: a first well 12 connected to a pad, fig. 1, to which an external pin is connected, the first well including a first-type diffusion region 18 that receives a well bias voltage, a second well 20 adjacent to the first well 12, a second well 20 including an insulating region 22 and at least one second-type diffusion region 30 outside the insulating region 22, fig. 1; and a third well 24 adjacent to the second well 20 and including a first-type diffusion region 28 that receives a first voltage, fig. 1, wherein the insulating region 22 inside the second well along with the first-type diffusion 18 region of the first well 12 constitute a bipolar junction transistor, which cuts off current flowing from the first well to the third well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure recited in the Tsuji's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes,

a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Regarding claim 12, Tsuji discloses a semiconductor device in fig. 1 comprising: a first N-well 12 connected to a pad to which an external pin is connected, the first N-well 12 including an N-type diffusion region 18 that receives a well bias voltage, and a P-type diffusion region 16, formed in the vicinity of the pad; a first P-well 20 adjacent to the first N-well 12, the first P-well 20 including an insulating region 22 and at least one P-type diffusion region 30 that receives a ground voltage outside the insulating region 22; and a second N-well 24 adjacent to the first P-well 20 and including an N-type diffusion region 28 that receives the ground voltage, wherein the insulating region 22 is a third N-well having an N-type diffusion region 26 that receives a control voltage, fig. 1.

Regarding claim 19, Tsuji discloses a method of forming a semiconductor device comprising: forming a first well 12 connected to a pad, fig. 1, to which an external pin is connected, the first well 12 including a first-type diffusion region 18 that receives a well bias voltage; forming a second well 20 adjacent to the first well 12, the second well 20 including an insulating region 22 and at least one second-type diffusion region 30 outside the insulating region 22; and forming a third well 24 adjacent to the second well 20 and including a first-type diffusion region 28 that receives a first voltage, wherein the insulating region 22 inside the second well 20 along with the first-type diffusion region 18 of the first well 12 constitute a bipolar junction transistor, fig. 1, which cuts off current flowing from the first well to the third well.

The recitation of 'cuts off current flowing from the first well to the third well.' is only a statement of the inherent properties of the product. The structure recited in the Tsuji's reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Or where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977) and MPEP 2112.01.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6690067 to Ker et al.

Regarding claims 11, 18, Kerr does not the semiconductor device wherein the third well 60 constitutes a depletion-type MOS transistor.

A recitation of 'a depletion-type MOS transistor' of the claimed invention does not result in a structural difference between the claimed invention and the prior art, thus claimed invention is only an art-recognized suitability for an intended purpose, MPEP 2144.07.

Response to Arguments

7. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
11 Oct. 2005